ANALOG DEVICES

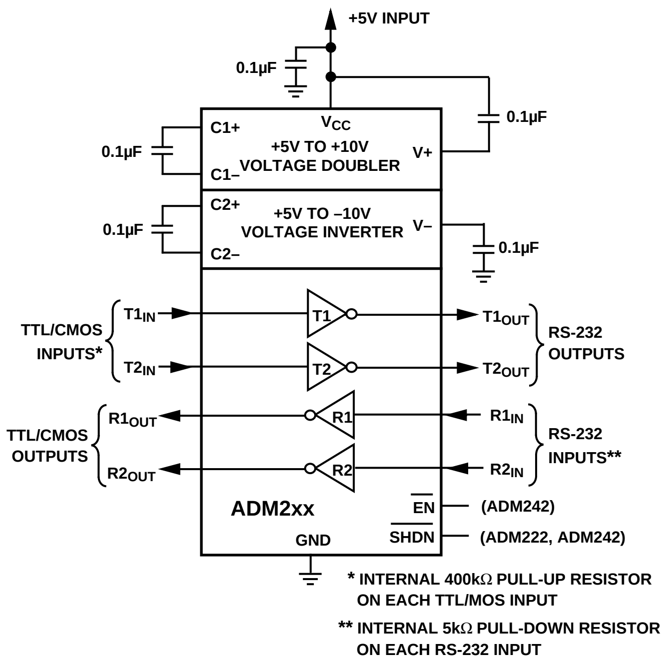
High Speed, +5 V, 0.1 μF CMOS RS-232 Drivers/Receivers

ADM222/ADM232A/ADM242*

FEATURES
200 kB/s Transmission Rate
Small (0.1 μF) Charge Pump Capacitors
Single 5 V Power Supply
Meets All EIA-232-E and V.28 Specifications
Two Drivers and Two Receivers
On-Board DC-DC Converters
±9 V Output Swing with +5 V Supply
±30 V Receiver Input Levels
Pin Compatible with MAX222/MAX232A/MAX242

APPLICATIONS
Computers
Peripherals
Modems
Printers
Instruments

FUNCTIONAL BLOCK DIAGRAM



ORDERING GUIDE

Model	Temperature Range	Package Option
ADM222AN	–40°C to +85°C	N-18
ADM222AR	–40°C to +85°C	R-18W
ADM232AAN	–40°C to +85°C	N-16
ADM232AARN	–40°C to +85°C	R-16N
ADM232AARW	–40°C to +85°C	R-16W
ADM242AN	–40°C to +85°C	N-18
ADM242AR	–40°C to +85°C	R-18W

GENERAL DESCRIPTION

The ADM222, ADM232A, ADM242 are a family of high speed RS-232 line drivers/receivers offering transmission rates up to 200 kB/s. Operating from a single +5 V power supply, a highly efficient on-chip charge pump using small (0.1 μF) external capacitors allows RS-232 bipolar levels to be developed. Two RS-232 drivers and two RS-232 receivers are provided on each device.

The devices are fabricated on BiCMOS, an advanced mixed technology process which combines low power CMOS with high speed bipolar circuitry. This allows for transmission rates up to 200 kB/s yet minimizes the quiescent power supply current to under 5 mA.

The ADM232A is a pin-compatible, high speed upgrade for the AD232 and for the ADM232L. It is available in 16-pin DIP and in both narrow and wide surface mount (SOIC) packages.

The ADM222 contains an additional shutdown ($\overline{SHDN}$) function which may be used to disable the device thereby reducing the supply current to 0.1 μA. During shutdown, all transmit/receive functions are disabled. The ADM222 is available in 18-pin DIP and in a wide surface mount (SOIC) package.

The ADM242 combines both shutdown ($\overline{SHDN}$) and enable ($\overline{EN}$) functions. The shutdown function reduces the supply curent to 0.1 mA. During shutdown, the transmitters are disabled but the receivers continue to operate normally. The enable function allows the receiver outputs to be disabled thereby facilitating sharing a common bus. The ADM242 is available in 18-pin DIP and in a wide surface mount (SOIC) package.

*Protected by U.S. Patent No. 5,237,209.

REV. 0

One Technology Way, P.O. Box 9106, Norwood. MA 02062-9106, U.S.A.
Tel: 617/329-4700 Fax: 617/326-8703

ADM222/ADM232A/ADM242–SPECIFICATIONS (V_{CC} = +5 V ± 10%, C1–C4 = 0.1 μF; all specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
RS-232 TRANSMITTERS					
Output Voltage Swing	±5	±9		V	All Transmitter Outputs Loaded with 3 kΩ to Ground
Input Logic Threshold Low, V_{INL}		1.4	0.8	V	T_{IN}
Input Logic Threshold High, V_{INH}	2.0	1.4		V	T_{IN}
Logic Pullup Current		5	40	μA	T_{IN} = 0 V
Data Rate	200			kB/s	
Output Resistance	300			Ω	V_{CC} = V+ = V– = 0 V, V_{OUT} = ±2 V
Output Short Circuit Current (Instantaneous)	±7	±22		mA	
RS-232 RECEIVERS					
RS-232 Input Voltage Range	–30		+30	V	
RS-232 Input Threshold Low	0.8	1.3		V	
RS-232 Input Threshold High		1.8	2.4	V	
RS-232 Input Hysteresis	0.2	0.5	1.0	V	V_{CC} = 5 V
RS-232 Input Resistance	3	5	7	kΩ	
TTL/CMOS Output Voltage Low, V_{OL}		0.2	0.4	V	I_{OUT} = 3.2 mA
TTL/CMOS Output Voltage High, V_{OH}	3.5			V	I_{OUT} = –1.0 mA
TTL/CMOS Output Short-Circuit Current	–2	–10		mA	Source Current (V_{OUT} = GND)
TTL/CMOS Output Short-Circuit Current	10	30		mA	Sink Current (V_{OUT} = V_{CC})
TTL/CMOS Output Leakage Current		±0.05	±10	μA	$\overline{SHDN}$ = GND/$\overline{EN}$ = V_{CC} 0 V ≤ V_{OUT} ≤ V_{CC}
$\overline{EN}$ Input Threshold Low, V_{INL}		1.4	0.8	V	
$\overline{EN}$ Input Threshold High, V_{INH}	2.0	1.4		V	
POWER SUPPLY					
Power Supply Current		4	8	mA	No Load
		15		mA	3 kΩ Load on Both Outputs
Shutdown Power Supply Current		0.1	10	μA	
$\overline{SHDN}$ Input Leakage Current			±1	μA	
$\overline{SHDN}$ Input Threshold Low, V_{INL}		1.4	0.8	V	
$\overline{SHDN}$ Input Threshold High, V_{INH}	2.0	1.4		V	
AC CHARACTERISTICS					
Transition Region Slew Rate	6	12	30	V/μs	C_L = 50 pF to 2500 pF, R_L = 3 kΩ to 7 k Ω Measured from +3 V to –3 V or –3 V to +3 V
Transmitter Propagation Delay TTL to RS-232		0.7	3.5	μs	t_{PHLT}
		0.7	3.5	μs	t_{PLHT}
Receiver Propagation Delay RS-232 to TTL		0.2	0.5	μs	t_{PHLR}
		0.3	0.5	μs	t_{PLHR}
Receiver Output Enable Time		125	500	ns	t_{ER}
Receiver Output Disable Time		160	500	ns	t_{DR}
Transmitter Output Enable Time		250		μs	$\overline{SHDN}$ Goes high
Transmitter Output Disable Time		3.5		μs	$\overline{SHDN}$ Goes low
Transmitter + to – Propagation Delay Difference		300		ns	
Receiver + to – Propagation Delay Difference		100		ns	

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{CC} . . . . +6 V
V+ . . . . (V_{CC} – 0.3 V) to +13 V
V– . . . . +0.3 V to –13 V
Input Voltages
T_{IN} . . . . –0.3 V to (V_{CC} + 0.3 V)
R_{IN} . . . . ±30 V
Output Voltages
T_{OUT} . . . . (V+, +0.3 V) to (V–, –0.3 V)
R_{OUT} . . . . –0.3 V to (V_{CC} + 0.3 V)
Short Circuit Duration
T_{OUT} . . . . Continuous
Power Dissipation N-16 . . . . 400 mW
(Derate 7.5 mW/°C above +70°C)
θ_{JA}, Thermal Impedance . . . . 80°C/W
Power Dissipation R-16N . . . . 400 mW
(Derate 7 mW/°C above +70°C)
θ_{JA}, Thermal Impedance . . . . 80°C/W
Power Dissipation R-16W . . . . 400 mW
(Derate 7 mW/°C above +70°C)
θ_{JA}, Thermal Impedance . . . . 80°C/W
Power Dissipation N-18 . . . . 400 mW
(Derate 7 mW/°C above +70°C)
θ_{JA}, Thermal Impedance . . . . 80°C/W
Power Dissipation R-18W . . . . 400 mW
(Derate 7 mW/°C above +70°C)
θ_{JA}, Thermal Impedance . . . . 80°C/W
Operating Temperature Range
Industrial (A Version) . . . . –40°C to +85°C
Storage Temperature Range . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . +300°C
Vapor Phase (60 sec) . . . . +215°C
Infrared (15 sec) . . . . +220°C

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Test Circuits

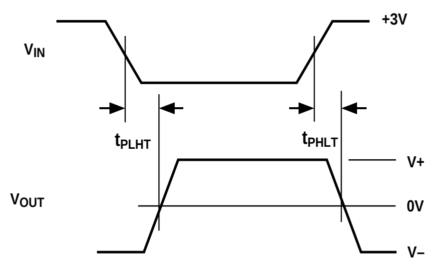


Figure 1. Transmitter Propagation Delay Timing

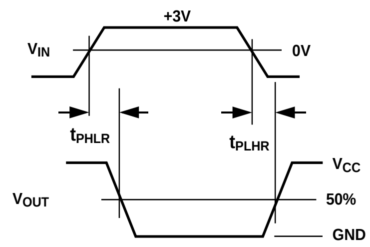


Figure 3. Receiver Propagation Delay Timing

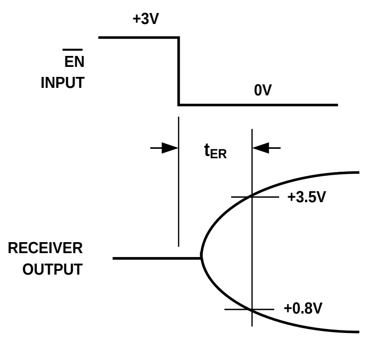


Figure 2. Receiver Enable Timing

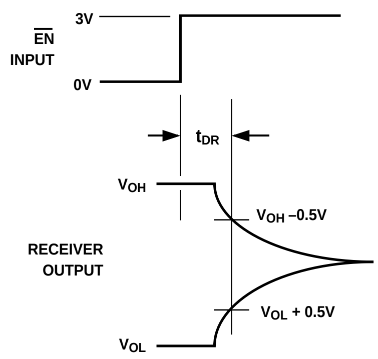


Figure 4. Receiver Disable Timing

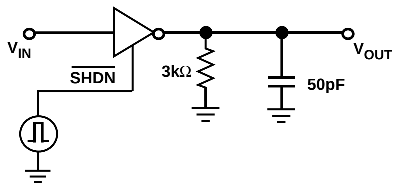


Figure 5. Shutdown Test Circuit

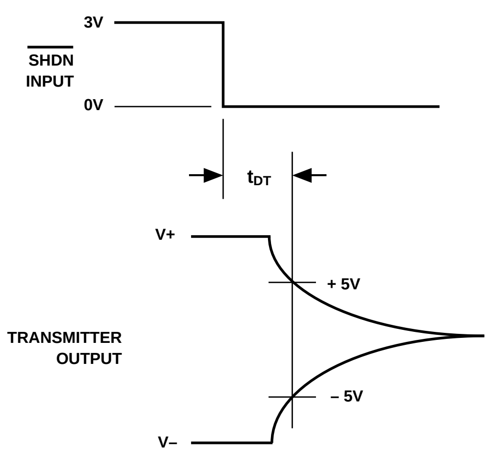


Figure 6. Transmitter Shutdown Disable Timing

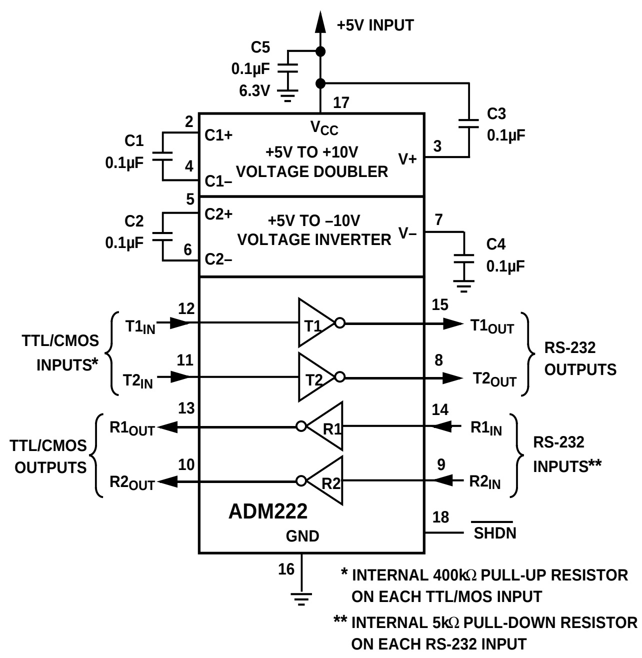


Figure 7. ADM222 Typical Operating Circuit

PIN FUNCTION DESCRIPTION

Mnemonic	Function
V_{CC}	Power Supply Input, +5 V ± 10%.
V+	Internally generated positive supply (+10 V nominal).
V–	Internally generated negative supply (–10 V nominal).
GND	Ground Pin. Must be connected to 0 V.
C1+	External capacitor 1, (+ terminal) is connected to this pin.
C1–	External capacitor 1, (– terminal) is connected to this pin.
C2+	External capacitor 2, (+ terminal) is connected to this pin.
C2–	External capacitor 2, (– terminal) is connected to this pin.
T_{IN}	Transmitter (Driver) Inputs. These inputs accept TTL/CMOS levels. An internal 400 kΩ pull-up resistor to V_{CC} is connected on each input.
T_{OUT}	Transmitter (Driver) Outputs. These are RS-232 levels (typically ±9 V).
R_{IN}	Receiver Inputs. These inputs accept RS-232 signal levels. An internal 5 kΩ pull-down resistor to GND is connected on each of these inputs.
R_{OUT}	Receiver Outputs. These are TTL/CMOS levels.
NC	No Connect. No connections are required to this pin.
$\overline{EN}$	(ADM242 Only) Active Low Digital Input. May be used to enable or disable (three-state) both receiver outputs.
$\overline{SHDN}$	(ADM222 & ADM242) Active Low Digital Input. May be used to disable the device so that the power consumption is minimized. On the ADM222 all drivers and receivers are disabled. On the ADM242 the drivers are disabled but the receivers remain enabled.

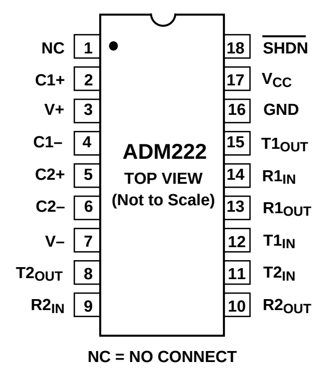


Figure 8. ADM222 DIP & SOIC Pin Configurations

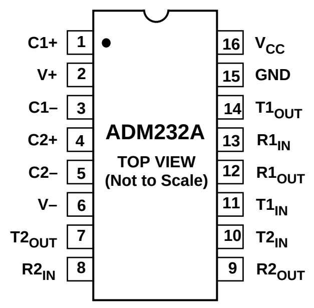


Figure 9. ADM232A DIP/SOIC Pin Configuration

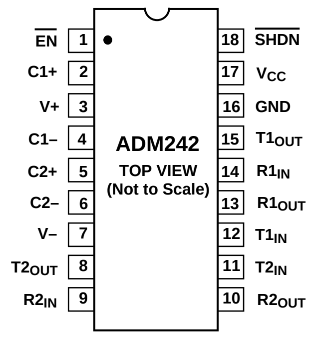


Figure 11. ADM242 DIP/SOIC Pin Configuration

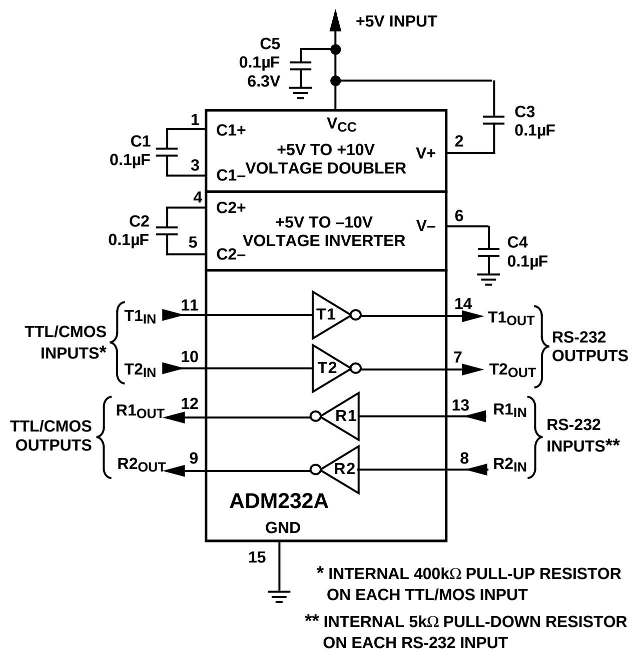


Figure 10. ADM232A Typical Operating Circuit

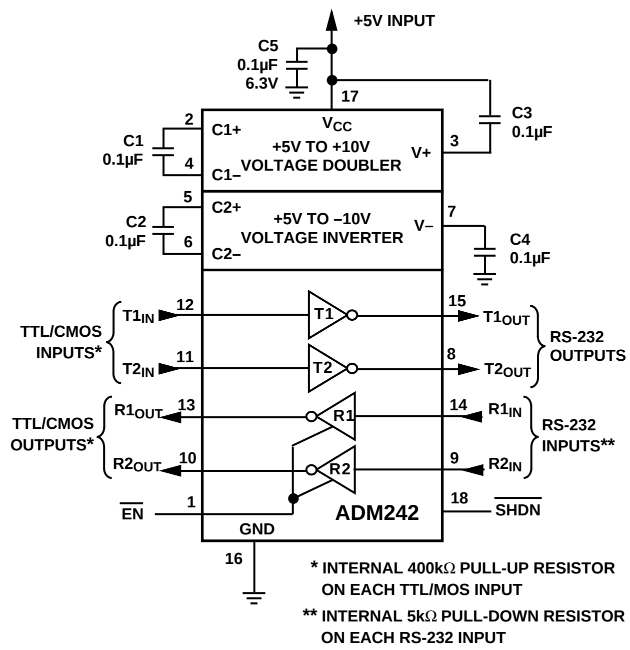


Figure 12. ADM242 Typical Operating Circuit

ADM222/ADM232A/ADM242–Typical Performance Characteristics

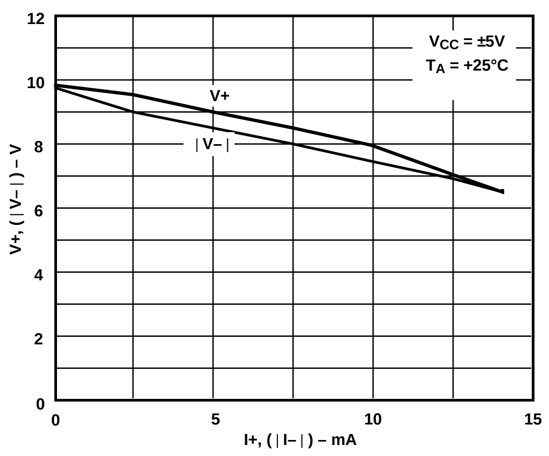


Figure 13. Charge Pump V+, V– vs. Current

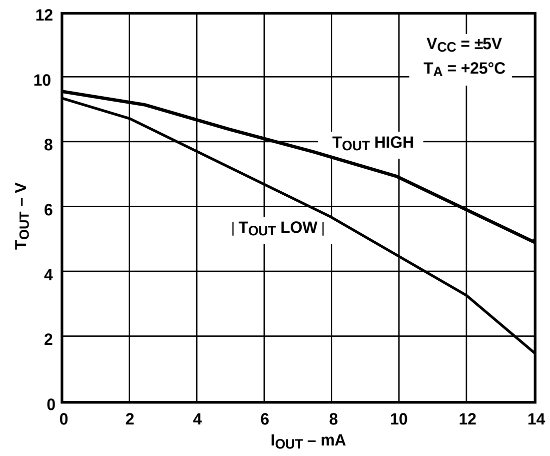


Figure 16. Transmitter Output Voltage vs. Current

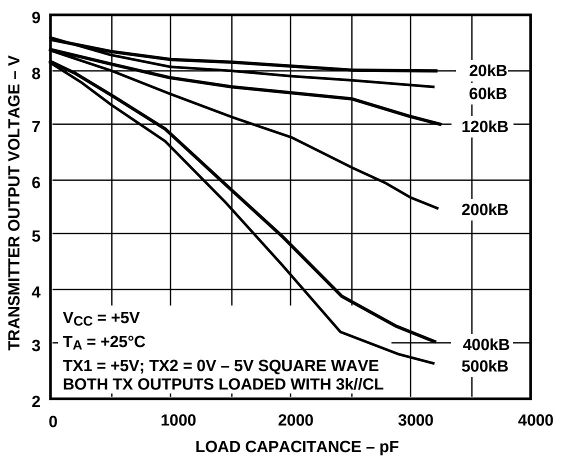


Figure 14. Transmitter Baud Rate vs. Load Capacitance

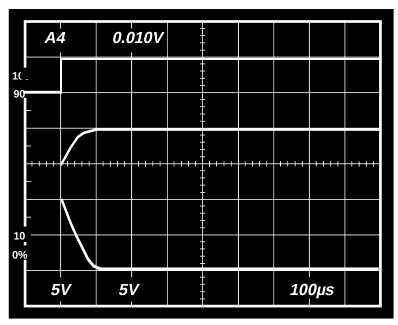


Figure 17. Charge Pump V+, V– Exiting Shutdown

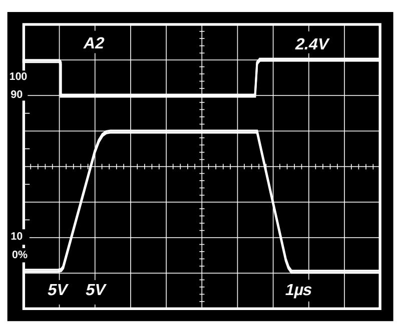


Figure 15. Transmitter Unloaded Slew Rate

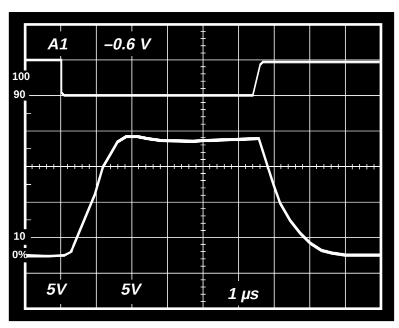


Figure 18. Transmitter Fully Loaded Slew Rate

GENERAL INFORMATION

The ADM222/ADM232A/ADM242 are high speed RS-232 drivers/receivers requiring a single digital +5 V supply. The RS-232 standard requires transmitters that will deliver ±5 V minimum on the transmission channel and receivers that can accept signal levels down to ±3 V. The parts achieve this by integrating step up voltage converters and level shifting transmitters and receivers onto the same chip. CMOS technology is used to keep the power dissipation to an absolute minimum. All devices contains an internal charge pump voltage doubler and a voltage inverter that generates ±10 V from the +5 V input. Four external 0.1 µF capacitors are required for the internal charge pump voltage converter.

The ADM222/ADM232A/ADM242 is a modification, enhancement and improvement to the AD230-AD241 family and derivatives thereof. It is essentially plug-in compatible and does not have materially different applications.

CIRCUIT DESCRIPTION

The internal circuitry consists of four main sections. These are:

A Charge Pump Voltage Converter
TTL/CMOS to RS-232 Transmitters
RS-232 to TTL/CMOS Receivers
Enable and Shutdown Functions.

Charge Pump DC-DC Voltage Converter

The Charge Pump Voltage converter consists of an oscillator and a switching matrix. The converter generates a ±10 V supply from the input 5 V level. This is done in two stages using a switched capacitor technique. The 5 V input supply is doubled to 10 V using capacitor C1 as the charge storage element. The –10 V level is also generated from the input 5 V supply using C1 and C2 as the storage elements.

Capacitors C3 and C4 are used to reduce the output ripple. Their values are not critical and can be reduced if higher levels of ripple are acceptable. The charge pump capacitors C1 and C2 may also be reduced at the expense of higher output impedance on the V+ and V– supplies.

The V+ and V– supplies may also be used to power external circuitry if the current requirements are small. Please refer to the typical performance characteristics which shows the V+, V– output voltage vs. current.

In the shutdown mode the charge pump is disabled and V+ decays to V_{CC} while V– decays to 0 V.

Transmitter (Driver) Section

The Drivers convert TTL/CMOS input levels into RS-232 output levels. With V_{CC} = +5 V and driving a typical RS-232 load, the output voltage swing is ±9 V. Even under worst case conditions the drivers are guaranteed to meet the ±5 V RS-232 minimum requirement.

The input threshold levels are both TTL and CMOS compatible with the switching threshold set at $V_{CC}/4$. With a nominal V_{CC} = 5 V the switching threshold is 1.25 V typical. Unused inputs may be left unconnected, as an internal 400 kΩ pull- up resistor pulls them high forcing the outputs into a low state.

As required by the RS-232 standard, the slew rate is limited to less than 30 V/µs without the need for an external slew limiting capacitor, and the output impedance in the power-off state is greater than 300 Ω.

Receiver Section

The receivers are inverting level shifters which accept RS-232 input levels (±3 V to ±15 V) and translate them into 5 V TTL/CMOS levels. The inputs have internal 5 kΩ pull-down resistors to ground and are also protected against overvoltages of up to ±30 V. The guaranteed switching thresholds are 0.8 V minimum and 2.4 V maximum which are well within the ±3 V RS-232 requirement. The low level threshold is deliberately positive as it ensures that an unconnected input will be interpreted as a low level.

The receivers have Schmitt trigger input with a hysteresis level of 0.5 V. This ensures error free-reception for both noisy inputs and for inputs with slow transition times

Enable and Shutdown Functions

On the ADM222, both receivers are fully disabled during shutdown.

On the ADM242, both receivers continue to operate normally. This function is useful for monitoring activity so that when it occurs, the device can be taken out of the shutdown mode.

The ADM242 also contains a receiver enable function ($\overline{EN}$) which can be used to fully disable the receivers, independent of $\overline{SHDN}$.

APPLICATIONS INFORMATION

A selection of typical operating circuits is shown in Figures 13 to 19.

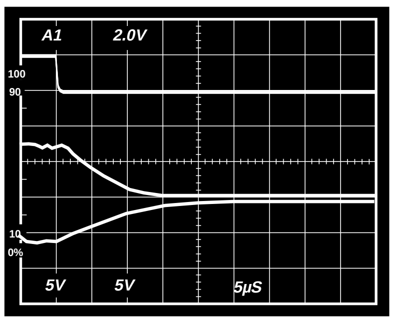
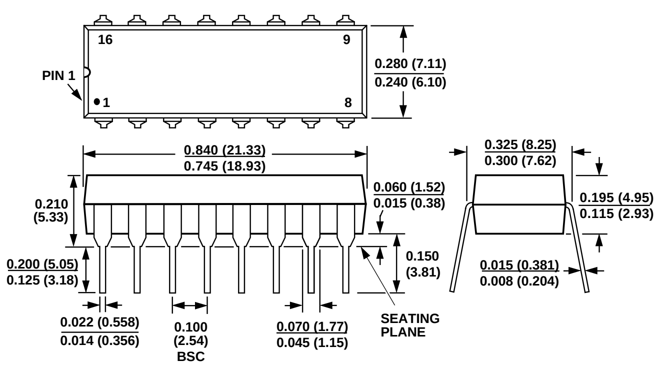


Figure 19. Transmitter Output Disable Timing

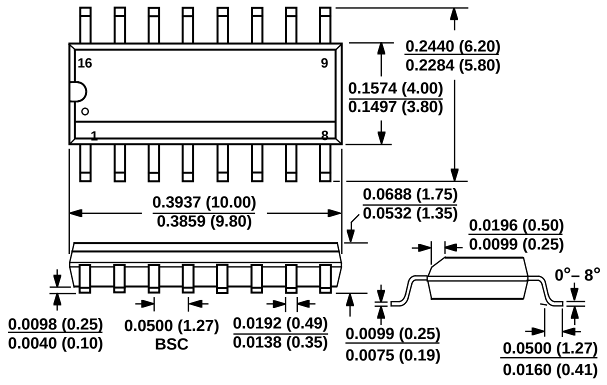
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

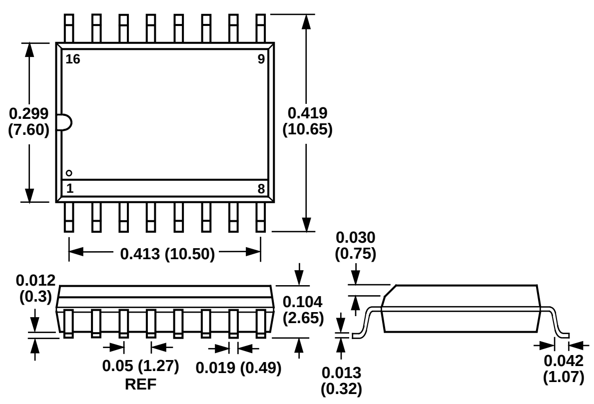
16-Pin Plastic DIP (N-16)



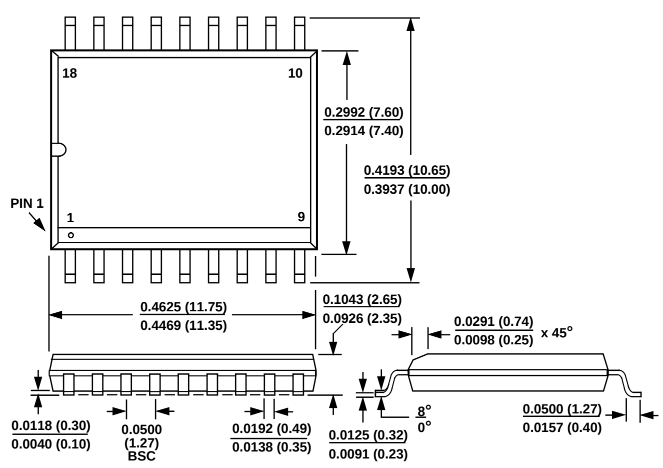
16-Lead Narrow SOIC (R-16N)



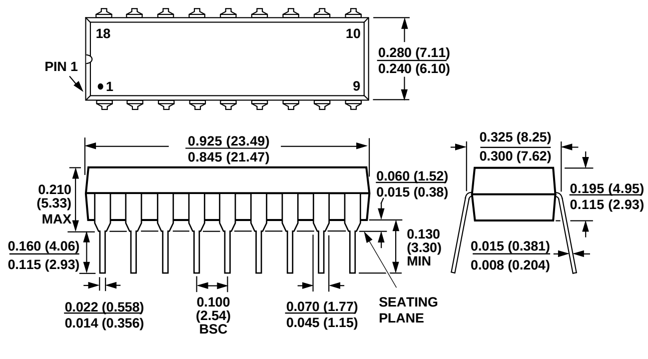
16-Lead Wide SOIC (R-16W)



18-Lead Wide SOIC (R-18W)



18-Pin Plastic DIP (N-18)



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ORDERING GUIDE

Model	Temperature Range	Package Option*
ADM222AN	–40°C to +85°C	N-18
ADM222AR	–40°C to +85°C	R-18W
ADM232AAN	–40°C to +85°C	N-16
ADM232AARN	–40°C to +85°C	R-16N
ADM232AARW	–40°C to +85°C	R-16W
ADM242AN	–40°C to +85°C	N-18
ADM242AR	–40°C to +85°C	R-18W

*For outline information see Package Information section.